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SUBSTITUTE SPECIFICATION

CONTROL CIRCUITS COMPARING INDEX OFFSET AND WAY FOR CACHE SYSTEM AND METHOD OF CONTROLLING CACHE SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a control circuit for controlling a cache system, and more particularly to a cache system control circuit having a store queue for temporary storing a store instruction and being capable of re-ordering the instructions.

2. Description of the Related Art

A semiconductor device may include a data cache or a data cache system and a store queue serving as a write buffer or a store buffer for data-write instruction or data store instruction. Data write operation to a main memory and data cache operation to a data memory may be made, wherein a store instruction including a write address and data is once held by the store queue for improvement in throughput of the processor. Those conventional techniques are disclosed in Japanese